Luke Neilson

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EXECUTIVE SUMMARY

Honors Electrical and Computer Engineering student specializing in digital logic, ASIC design, and computer architecture. Proven ability to deliver elite results in high-pressure environments, managing rigorous safety and production demands. Seeking to leverage expertise in SystemVerilog, RTL design, and custom hardware acceleration for advanced digital circuit development.

EDUCATION

Oregon State University Honors College **Expected June 2027**
H.B.S. Electrical & Computer Engineering (Accelerated M.S. Track) *GPA: 3.92*
- Awards: Drucilla Shepard Smith Award (4.0), Tau Beta Pi Engineering Honor Society

RELEVANT TECHNICAL SKILLS

Hardware & Architecture
ASIC Design, FPGA, MIPS Architecture, Mixed-Signal Circuit Design

Languages
SystemVerilog, Verilog, C, C++, AVR Assembly, Bash/Shell

Software & Tools
Cadence Xcelium, Cadence Genus, Intel 22nm PDK, Quartus, ModelSim, Vivado

ENGINEERING & LEADERSHIP EXPERIENCE

Brain-Inspired Computing Lab (OSU) **Current**
Undergraduate Researcher *Corvallis, OR*
- Designing and synthesizing highly hardware-efficient Leaky Integrate-and-Fire neuron models.
- Engineered RTL architecture in SystemVerilog, replacing expensive multiplier-based leakage decay with highly efficient arithmetic right bit-shift operations.

Mortenson **Summer 2026**
Electrical Engineering Intern *Oklahoma*
- Served as the primary coordinator for two subcontractors while managing a complex decommissioning scope.
- Executed work in 72+ hour weeks, maintaining extreme focus where safety was paramount alongside intense pressure for production and quality.

Division I Men's Rowing (OSU) **2024 – 2025**
Varsity Rower *Corvallis, OR*
- Walked on with zero prior experience, advancing to the Varsity roster to compete at IRA National Championships.
- Maintained a rigorous 20+ hour/week training schedule while earning a 3.9+ GPA in Honors ECE.

ARCHITECTURE & DIGITAL LOGIC PROJECTS

Spiking Neural Network (SNN) Hardware Optimization
- Achieved a highly optimized Power, Performance, and Area (PPA) footprint consisting of 0 multiplier/DSP blocks, 17 sequential registers, and 162 combinational cells for a total area of ~96.7 μm^2.

AES-128 Hardware Cryptography Module
- Designed and simulated a custom implementation of the AES-128 encryption algorithm using Verilog and Digital Logic.

Matrix Multiplication Hardware Accelerator
- Developed a hardware accelerator for matrix multiplication using Verilog, documented as a potential curriculum assignment for ECE474/574.

Dual-Channel 34MSa/s Oscilloscope
- Co-designed a custom mixed-signal PCB from the ground up, achieving a 34MSa/s sampling rate that shattered the previous university course record of 3MSa/s.
- Engineered high-speed data acquisition using an NXP LPC4370, addressing complex signal integrity, memory buffering, and precise clock timing challenges.